REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 1-18 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over the combination of applicants' admitted prior art ("AAPA") in view of U.S. Patent No. 5,177,567 to Klersy, et al. ("Klersy, et al.") and further in view of ADEL S. SEDRA & KENNETH C. SMITH, MICROELECTRONIC CIRCUITS (4TH Ed 1998)("Sedra and Smith"). Claims 2 and 5-8 stand rejected under 35 U.S.C. 103(a) as allegedly obvious over the combination of the AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 6,331,492 to Misium, et al. ("Misium, et al."). Claims 3, 4, 16, and 17 stand rejected under 35 U.S.C. §103(a) as allegedly obvious over the combination of the AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 4,987,102 to Nguyen, et al. ("Nguyen, et al."). Claims 10 and 11 stand rejected under 35 U.S.C. §101(a) as allegedly obvious over the combination of the AAPA, Klersy, et al., Sedra and Smith, and U.S. Patent No. 4,757,027 to Vora, et al. ("Vora, et al."). Claim 12 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over the combination of the AAPA, Sedra and Smith, and U.S. Patent No. 6,268,779 to Van Zeijl ("Van Zeijl").

Applicants observe that in the second-fifth obviousness rejections the Examiner referred to a Hasegawa reference. Applicants have reviewed their file, but cannot find any Hasegawa reference that is of record in this case. It appears that the Klersy, et al. reference was meant to be included with the second-fifth obviousness rejections. Thus, applicants have included that reference with those rejections. In the event that a

Hasegawa reference was intended to be applied, applicants respectfully request that a proper citation with a copy of the Hasegawa reference be supplied in the next Office Action, which should be a non-final one because of the above omission.

Applicants submit that Claims 1-18 of the present application are not obvious from the applied references or the AAPA since none of the references teaches or suggests applicants' claimed method or structure which includes providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in the insulator layer. A permanent conformal passivation layer is then formed on the exposed sidewalls of the emitter, insulator layer, and a portion of the SiGe base regions. The exposed silicon regions not covered by the permanent conformal passivation layer are then silicided.

Applicants submit that the primary reference, the AAPA as depicted in FIG. 1, fails to teach or suggest a permanent conformal passivation layer formed on the exposed sidewalls of an emitter region. The AAPA discloses a heterojunction bipolar transistor structure, which does not include a conformal passivation layer. The heterojunction bipolar transistor structure, as disclosed in the AAPA, typically results in a 20-30% bipolar yield loss. The loss associated with the SiGe bipolar transistor structure, as disclosed in the AAPA, is attributed to the presence of silicide bridges between the emitter and SiGe body, which introduce shorts to the structure during silicidation. Applicants' claimed method and structure utilize a permanent conformal passivation

layer to avoid the formation of silicide bridges and losses associated with prior art devices.

The above deficiencies in the AAPA are not alleviated by the disclosure of Klersy, et al. since the applied reference does not teach or suggest a bipolar transistor structure including a permanent conformal passivation layer positioned on the *exposed sidewalls of an emitter*, a patterned insulator layer and a portion of a SiGe base region; and silicide regions which are located on exposed portions of a SiGe layer, including portions of the SiGe base region and the emitter not covered by the permanent conformal passivation layer.

The Klersy, et al. device is far removed from applicants' bipolar transistor. A bipolar transistor is a three terminal device having emitter, base and collector regions, where each region is in intimate contact with a separate terminal through which voltage is applied. Klersy, et al. disclose an electrical switching device fabricated of a chalcogenide material. The switching device disclosed in Klersy, et al. is a two terminal device where current flow is dictated by the chalcogenide body separating the first electrode (first terminal) and a second electrode (second terminal). The device disclosed in Klersy, et al. does not include an emitter region. Therefore, since Klersy, et al. fail to teach or suggest an emitter region, Klersy, et al. fail to teach or suggest *a passivation layer formed on the exposed sidewalls of an emitter*, as recited in Claims 1, 9 and 18.

It is the Examiner's position, referring to page 3 of the present Office Action, that it would have been obvious for one of ordinary skill in the art to modify the AAPA with the passivation layer disclosed in Klersy, et al., since it is well known within the art that for a transistor to be useable it should not be shorted between the base and the emitter.

Applicants' submit that there is no motivation for one of ordinary skill in the art to modify a three terminal bipolar transistor to include a passivation layer utilized in a two terminal chalcogenide switching device because chalcogenide devices and bipolar transistors are not within the same field of endeavor and the Klersy, et al. reference is not reasonably pertinent to the problem in which applicants' were concerned. *See In re Oetiker,* 977 F.2d 1443, 1446 24 USPQ2d 1443, 1445 (Fed. Cir 1992).

Applicants note that the present invention and the Klersy, et al. device both present switching devices, but submit the test for analogy is not simple classifications of devices, but whether the similarities and differences in the structure and function of the devices indicate whether referenced patents where pertinent to the art in which the applicants' invention dealt. *In re Ellis,* 476 F.2d 1370, 1372, 177 USPQ 526, 527, (CCPA 1973).

The court in *Wang Laboratories, Inc. v. Toshiba Corp.* 993 F.2d 185, 26 USPQ2d 1767 (Fed. Cir. 1993) held that a prior art reference to single in-line memory modules for installation in industrial controllers were not necessarily in the same field of endeavor as patent claims directed to single in-line memory modules for installation on printed circuit motherboards for use in personal computers. The court reasoned that the reference was in a different field of endeavor because it involved memory circuits in which modules of varying sizes may be added or replaced, whereas the claimed invention included compact modular memories. Additionally, the Federal Circuit reasoned that a holding of non-analogous art was supported by the fact that the claims for the single in line memory modules at issue utilized dynamic random access memory, where the single in-line memory modules of the prior art reference utilized static random access memories or read

only memories. Dynamic random access memory and static random access or read only memories have differing structure and function.

The claimed bipolar transistor and the switching device disclosed in Klersy, et al. are non-analogous art. Similar to the devices considered by the Federal Circuit in *Wang Laboratories, Inc. v. Toshiba Corp.*, the claimed bipolar transistor and the chalcogenide switching device disclosed in Klersy, et al. have differing structure and function. As discussed above, a bipolar transistor comprises an emitter, base and collector and is a three terminal device, where the interaction between the emitter and base and their respective terminals control the switching behavior of the device and provide multiple conduction states. An efficient bipolar transistor has an emitter region having a higher doping concentration than the base region and a base region having a higher doping concentration than the collector. In order for the bipolar transistor to switch 'on', and for current to flow across the emitter/base junction the voltage introduced to the base region (p-type base in pnp transistor) must cause the potential of the base region to be greater than the potential of the emitter region, thus forward biasing the emitter base junction.

The chalcogenide switching device disclosed in Klersy, et al. does not have the doped emitter, base and collector regions of a bipolar transistor. Klersy, et al. disclose a two terminal device in which the terminals are separated by a chalcogenide body, where the electrical properties of the chalcogenide material provide switching behavior. The switching behavior of the device disclosed in Klersy, et al. is controlled by the voltage applied to the chalcogenide body through a first terminal. When enough voltage is applied, the chalcogenide body switches from a non-conductive state to a conductive state allowing current to flow from the first terminal through the chalcogenide body to a

second terminal. The Kersly, et al. device, contrary to applicants' claimed bipolar transistor, has only two states of conduction, where the device does not conduct or is highly conductive depending on the voltage applied to the chalcogenide body. The Klersy, et al. device is far removed from applicants' claimed bipolar transistor.

Applicants' claimed bipolar transistor and the chalcogenide switching device disclosed in Klersy, et al., similar to the technology discussed by the Federal Circuit in *Wang Laboratories, Inc. v. Toshiba Corp.*, have a substantially different structure and substantially different functionality indicating that the applied reference and applicants' claimed structure pertain to non-analogous art. Therefore, since the applied reference pertains to non-analogous art, there is no motivation to modify AAPA with the passivation layer disclosed in Klersy et al. in a manner to produce applicants' claimed bipolar transistor structure.

Applicants' further note that Klersy, et al. is not reasonably pertinent to the problem in which applicants' were concerned. Applicants disclose that the positioning of the passivation layer on the exposed sidewalls of the emitter reduces the incidence of emitter/base shorts formed during silicidation of the exposed surfaces of the bipolar transistor. Shorting the emitter region to the base region produces a transistor that will not switch on, because when the emitter region and base region are in intimate electrical contact the potential of the base region cannot be greater than the emitter region. Therefore, shorting the base and emitter produces a device that does not provide current flow.

In addition to failing to teach or suggest a bipolar transistor including an emitter region, Klersy, et al. also fail to disclose silicide formation or the incidence of silicide

shorts resulting in a device that will not switch on. The short circuit disclosed in Klersy, et al. occurs where the chalcogenide body is bypassed through a low resistance conduction path introduced by contamination from the first and second terminals. Opposite the problem in which applicants' were concerned, current flow that bypasses the chalcogenide body produces a device that is effectively switched on resulting in an uncontrolled high current between the terminals. Therefore, since the problem considered by Klersy, et al., where a short circuit results in a device with an uncontrolled high current flow, is opposite the problem considered by applicants, where a short produces a device that will not switch on and will not flow current, Klersy, et al. are not reasonably pertinent to the problem in which applicants' were concerned. Since Klersy, et al. are not pertinent to the problem in which applicants' were concerned, there is no motivation to modify or combine the passivation layer disclosed in Klersy, et al. in a manner to produce the applicants' claimed structure.

Klersy, et al. also fail to teach or suggest applicants' method as recited in Claim 1. Claim 1 recites providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls; *forming a permanent passivation layer on said exposed sidewalls of said emitter*, said insulator layer and portions of said SiGe base region; and siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein. Applicants further

disclose that the formation of the passivation layer on the sidewall of the emitter reduces the number of shorts between the emitter and base during the passivation process.

Applicants submit that Klersy, et al. do not teach or suggest *forming a permanent passivation layer on said exposed sidewalls of said emitter, said insulator layer and portions of said SiGe base region; and siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said permanent passivation layer to form silicide regions therein.* Klersy, et al. do not disclose forming silicide regions, nor recognize the introduction of shorts during the silicide process. Additionally, the order of processing steps disclosed in Klersy, et al. teach away from forming the insulating layer 6 on the exposed sidewalls of the emitter prior to silicidation in a manner that would decrease the incidence of base/emitter shorts. The method disclosed in Klersy, et al. first forms a lower electrode on a substrate and then deposits an insulating layer 6. An opening is then formed in the insulating layer where the chalcogenide body is positioned in contact with the lower electrode. Thereafter, the upper electrode is then positioned atop the chalcogenide body. Therefore, since the insulating layer 6 (passivation layer) is formed prior to the chalcogenide body, it is not formed on the exposed regions of the device and would not reduce the incidence of shorts produced during silicidation. Klersy, et al. do not teach or suggest the applicants' claimed method.

Sedra and Smith do not fulfill the deficiencies of the AAPA and the Klersy, et al. reference. Sedra and Smith, referring to page 222, disclose a bipolar junction transistor consisting of three semiconductor regions; the emitter, the base region, and the collector region. Sedra and Smith fail to teach or suggest *a permanent passivation layer on said exposed sidewalls of said emitter* as recited in Claims 1, 9 and 18.

Misium, et al. do not fulfill the deficiencies of the combined disclosures of the AAPA, Sedra and Smith and Klersy, et al. Misium, et al., referring to Column 3 lines 49-53, are directed to a process for rending a silicon dioxide layer resistant to etch chemistries used in integrated circuit component manufacturing, such as HF. Misium, et al. fail to teach or suggest *a permanent passivation layer on exposed sidewalls of an emitter, or forming a permanent passivation layer on the exposed sidewalls of an emitter*, as recited in Claims 1, 9 and 18.

Nguyen, et al. do not fulfill the deficiencies of the combined disclosures of AAPA, Sedra and Smith, and Klersy, et al. Nguyen, et al. disclose a method for forming high purity thin films on a semiconductor substrate, where the preferred method of thin film deposition is plasma enhanced chemical vapor deposition. Nguyen, et al. fail to teach or suggest *a permanent passivation layer on exposed sidewalls of an emitter, or forming a permanent passivation layer on the exposed sidewalls of an emitter* as recited in Claims 1, 9 and 18.

Vora, et al. do not fulfill the deficiencies of the combined disclosures of AAPA, Sedra and Smith, and Klersy et al. Vora, et al. relate to techniques for making vertical transistor structures in islands of an epitaxial silicon layer. Vora, et al. fail to teach or suggest *a permanent passivation layer on exposed sidewalls of an emitter, or forming a permanent passivation layer on the exposed sidewalls of an emitter* as recited in Claims 1, 9 and 18.

Van Zeijl does not fulfill the deficiencies of the combined disclosures of the AAPA, Sedra and Smith, and Klersy et al. Van Zeijl relates to an integrated voltage controlled oscillator including varacitors and fixed capacitors in a stacked arrangement.

where the stacked arrangement decreases the surface area required for implementation of the device. Van Zeijl fails to teach or suggest *a permanent passivation layer or forming a permanent passivation layer on the exposed sidewalls of an emitter* as recited in Claims 1, 9 and 18.

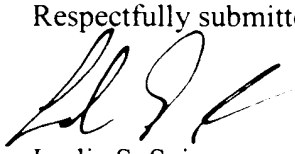
The §103 rejections also fail because there is no motivation to modify the prior art structures to include applicants' claimed method and structure, where a permanent passivation layer defines the locations where silicide regions contact the SiGe layer and surface of the emitter, as recited in Claims 1, 9 and 18. The §103 rejection is thus improper since the prior art does not suggest this dramatic modification.

The law requires that a prior art reference provide some teaching, suggestion or motivation to make the modification. In re Vaeck, 947 F.2d 488, 493, 20 USPQ 2d 1438, 1442 (Fed. Cir. 1991). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. "In re Fritch, 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

There is no suggestion in the prior art of applicants' claimed method or structure recited in pending Claims 1-18. As such, the claims of the instant application are not obvious from any of the above-mentioned prior art references. Therefore, applicants respectfully submit that the rejection under 35 U.S.C. §103 has been obviated; and the withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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